REMARKS

Claims 1-37 are pending in the application.

Claims 1-11 and 17-32 are rejected.

Claims 12-16 are objected to.

Claims 1, 8, 19-21, and 28 have been amended.

Claims 33-37 have been added.

Objection to the Drawings

FIG. 1B was objected to in the Office Action because all blocks were not labeled with descriptive legends. Submitted with this response is a proposed drawing change, which shows a revised FIG. 1B in which the previously unlabeled interconnections between nodes have been given reference number 194. The paragraph beginning on line 13 of page 8 and ending on line 24 of page 8 has also been amended to refer to this reference number.

FIGs. 1B-3, 5, 6, 10, 11, 14, 14, and 19 were objected to by the Draftsperson's Patent Drawing Review as having incorrect left drawing margins. Proposed replacement sheets of these drawings are submitted with this response.

Incorporation by Reference

The specification has been amended to include the serial numbers and filing dates of the applications incorporated by reference in the cross-references to related applications. With respect to "GR-253: Synchronous Optical Network (SONET) Transport Systems, Common Generic Criteria, Issue 2," Applicants note that this reference provides non-essential material indicating the state of the art. As such, Applicants are not required to provide a copy of this reference in order for the incorporation by reference to be proper.

Objections to the Claims

Claims 1, 8, 19, 20, 21, and 28 were objected to due to various informalities. These claims have been amended to correct these informalities.

Rejection of Claims under 35 U.S.C. §112

Claims 1, 9, 18, 19 and 25-28 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. These claims have been amended to provide correct antecedent basis.

Claims 9, 18, 19 and 25-27 were rejected under 35 U.S.C. §112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements.

With respect to the asserted omission of a "phase-locked loop" from the specification, Applicants have amended the paragraph beginning on line 25 of page 25 of the specification to include the statement: "In some embodiments, the clock and data recovery unit may include a phase-locked loop." Since claim 9 is part of the disclosure, as originally filed, this amendment does not add new matter. See *In re Benno*, 768 F.2d 1340, 226 USPQ 683 (Fed. Cir. 1985) and MPEP 2163.06(III). Applicants assert that this element is properly interrelated to the other elements of claim 9 and respectfully request withdrawal of the rejection.

With respect to the asserted omission of a "parity checker" from the specification, Applicants note that p. 25, lines 15-17 of the specification states: "Error checker 900 can be, for example, one of a number of different types of parity generators." Applicants assert that this provides proper support for the claims 18 and 25. Applicants also assert that the recited "parity checker" is properly interrelated to the other claim elements as required by 35 U.S.C. 112, second paragraph and respectfully request withdrawal of the rejection.

Applicants have amended the paragraph beginning on line 1 of page 5 of the specification to state: "each frame may contains an error check entry, and the error checker may generate error check information by analyzing one of the frames and comparing a result of said analyzing to an error check entry of another frame." Since claim 19 is part of the original disclosure, this amendment does not add new matter. Applicants assert that the recited "error check entry" is

properly interrelated to the other claim elements of claim 19 and respectfully request withdrawal of the 35 U.S.C. §112 rejection.

Applicants have amended the to state: "error checker 900 may be configured to receive several frames in a sequence, to generate parity information for a currently-processed frame of those frames, where the currently-processed frame occurs at a particular position in the sequence, and to compare the parity information to a parity entry in another one of the frames. In one embodiment, each of the frames is a SONET frame, the parity entry is a B1 byte of a SONET frame, and the other one of the frames is at another position in the sequence that is immediately subsequent to the position in said sequence." Since claims 26 and 27 are part of the original disclosure, this amendment does not add new matter. Applicants assert that the recited "parity entry" is properly interrelated to the other claim elements of claim 26. Similarly, the recited "B1 byte" is properly interrelated to the other claim elements of claim 27. Accordingly, Applicants respectfully request withdrawal of the 35 U.S.C. §112 rejection.

Rejection of Claims under 35 U.S.C. §103

Claims 1-5, 20-21 and 28-30 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yoshifuji, U.S. Patent 5,917,426, in view of Bala et al., U.S. Patent 6,307,653.

With respect to claim 1, the cited art fails to teach or suggest a signal router comprising: a switching matrix, where the switching matrix has a first number of inputs and a second number of outputs; and an error detector, coupled to one of said second number of outputs and configured to generate error information by virtue of being configured to detect errors in an information stream, where the switching matrix is configured to receive the information stream at the one of the first number of inputs.

Yoshifuji teaches a method involving "connecting a selected one of the input terminals to a selected one of the output terminals through the switch matrix by the use of the connection data signals, monitoring the connection state of the switch matrix, obtaining actual interconnection data signals from the connection state of the switch matrix, and substituting the actual interconnection data signals for the connection data signals when any disorder takes place in

connection with the connection data signals." Yoshifuji, col. 1, line 64 – col. 2, line 4. Thus, Yoshifuji teaches substituting the actual interconnection data signals obtained from the connection state for the connection data signals in response to a disorder in the connection data signals, which control the interconnection of input and output terminals. Applicants note that the connection data signals in Yoshifuji are not an information stream received by one of a first number of inputs of a switching matrix.

Bala, both alone and in combination with Yoshifuji, also fails to teach or suggest a signal router that includes a switching matrix having an error detector configured to detect errors in an information stream received at one of the first number of inputs of the switching matrix. In Bala, the "additional output port of the 2x2 optical switches can be used to monitor signal levels before putting a signal on the intended output line." Bala, col. 4, lines 47-49. Thus, in Bala, an output of an optical switch can be monitored to determine the signal level at that optical output. However, monitoring an optical signal level does not teach or suggest detecting errors in an information stream received by one of a first number of inputs of a switching matrix. For example, merely knowing the strength of an optical signal does not allow a determination regarding whether the information being conveyed by that signal contains any errors. Additionally, the combination of Bala and Yoshifuji also fails to teach the claimed invention. The combination of the two references, at best, suggests monitoring optical signal levels at the output of an optical switch and monitoring connection data signals that control how an input terminal is connected to an output terminal. This combination fails to teach or suggest an error detector coupled to the output of a switching matrix that is configured to detect errors in an information stream received by one of a first number of inputs of the switching matrix, as recited in claim 1. For at least this reason, claim 1 is patentable over the cited art.

Claims 2-5 depend from claim 1. These claims are patentable over the cited art for at least the foregoing reasons provided above with respect to claim 1. Claims 20-21 and 28-30 are patentable over the cited art for similar reasons.

Further with respect to claim 5, the cited art fails to teach or suggest a controller that further configures the switching matrix to couple the one of the first number of inputs to another

of the second number of outputs in addition to the one of the second number of outputs. The Office Action cites Yoshifuji as teaching a system configured to change or reconfigure the connection path. Similarly, the Office Action states that "Bala also discloses the optical switch re-routes the link path." Office Action, p. 7. However, reconfiguring or rerouting a connection path simply decouples one output from a particular input and then couples a different output to that input. In contrast, claim 5 recites coupling two outputs to the input ("to couple the one of the first number of inputs to another of the second number of outputs in addition to the one of the second number of outputs"). Applicants note that this feature of claim 5 may, in at least some embodiments, allow an information stream to be checked for errors via one output without disrupting the information stream as the information stream is also being transmitted via another output. This may in turn support error checking in an information stream being conveyed via a non-blocking switching matrix. None of the cited art teaches or suggests such a feature. Accordingly, claim 5 is patentable over the cited art for at least this reason. Claims 21 and 30 are patentable over the cited art for similar reasons.

Claims 6-9, 22 and 31 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yoshifuji, U.S. Patent 5,917,426, in view of Bala et al., U.S. Patent 6,307,653, and further in view of Al-Salameh, U.S. Patent 6,262,820. Claims 6-9 are patentable over the cited art for at least the reasons given above with respect to claim 1. Claims 22 and 31 are patentable over the cited art for similar reasons.

Claims 10-11, 17-19, 23-27, and 32 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yoshifuji in view of Bala and further in view of Maezawa et al., U.S. Patent 6,145,024. Claims 10-11 and 17-19 are patentable over the cited art for at least the reasons provided above with respect to claim 1. Claims 23-27 and 32 are patentable over the cited art for similar reasons.

Allowable Claims

Claims 12-16 were objected to as being dependent on a rejected base claim and indicated as being allowable if rewritten to overcome the 35 U.S.C. §112, second paragraph rejections and to include all of the limitations of the base claim and any intervening claims. Claims 33-37 are

substantially similarly to claims 12-16, rewritten in independent form, and thus claims 33-37 are believed to be allowable. Claims 12-16 are allowable due to their dependence on an allowable base claim.

Information Disclosure Statement

Applicants submitted an Information Disclosure Statement and accompanying Form PT-1449 on March 24, 2003. Applicants respectfully request the Examiner to carefully consider the listed references and return a copy of the signed and initialed Form PTO-1449.

CONCLUSION

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephone interview, the Examiner is invited to telephone the undersigned at 512-439-5080.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on July 17, 2003.

Brenna A Brock — Attorney for Applicant(s)

July 17, 2003 — Date of Signature

Respectfully submitted,

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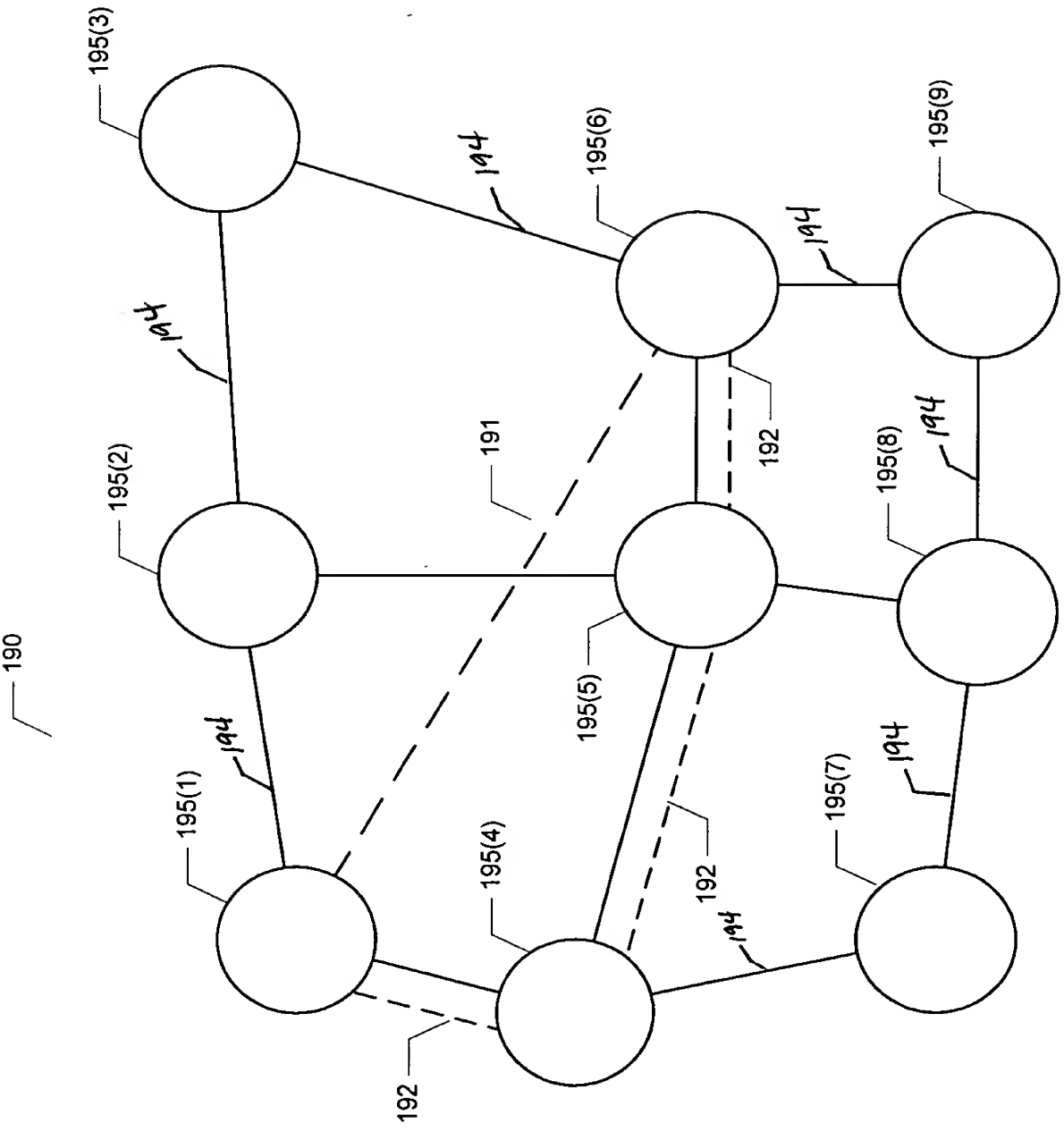

Fig. 1B